**Amendment to the Claims**

21. (twice amended) A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming a plurality of gate trenches extending from the upper surface of said upper layer through said well region to said drain region;

(e) forming sidewalls and floor in each trench comprising a layer of dielectric material;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material,

(g) removing said trench mask from the upper surface of said upper layer [and leaving the sidewall isolation layer in place];

(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and within said gate trench [and on said sidewall isolation layer], said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is substantially coplanar with the upper surface of said upper layer,

(j) forming a plurality of heavily doped source regions having a second polarity in said well region, said source regions extending to a selected depth from the upper surface of said upper layer where said selected depth is substantially coplanar with the level of the conductive gate material in the trench, <u>said step of forming comprising implanting the entire upper surface of said substrate with a ions of said second polarity, then forming a body mask on the upper surface of said substrate, said mask comprising openings transverse to said trenches</u>;

(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer, <u>said step of forming comprising doping the upper surface of said substrate with a dopant of said first polarity, then removing said body mask</u>; and

(1) forming a metal contact to said body and source regions over the upper surface of said upper layer.

22. (original) The process of claim 21 wherein said substrate comprises monocrystalline silicon.

23. (original) The process of claim 21 wherein said upper layer comprises an epitaxial layer.

Cancel claim 24.

25. (previously amended) The process of claim 21 wherein said source regions surround said body regions and the source regions are separated from each other by trenches.

26. Cancelled.

27. Cancelled.

28. Cancelled

29. Cancelled.

30. Cancelled.

31. Cancelled.

32. Cancelled.

33. Cancelled.

34. (original) The process of claim 21 wherein said dielectric material forming said sidewalls, said floor, and said isolation layer in said gate trench comprises silicon dioxide

35. (original) The process of claim 21 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon.

36. (original) The process of claim 21 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer.

37. (previously amended) The process of claim 21 wherein said first polarity is P and said second polarity is N.

38. (previously amended) The process of claim 21 wherein said first polarity is N and said second polarity is P.

39. (original) The process of claim 21 wherein said device is selected from the group consisting of a power MOSFET, an insulated gate bipolar transistor, an MOS-controlled thyristor, and an accumulation FET.

40. (original) A process for forming an improved trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;

(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;

(c) forming a gate trench mask on said upper surface of said upper layer;

(d) forming a plurality of gate trenches extending from the upper surface of said upper layer through said well region to said drain region;

(e) forming sidewalls and floor in each trench comprising a layer of [undoped] dielectric material;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material,

(g) removing said trench mask from the upper surface of said upper layer;

(h) forming an isolation layer of [undoped] dielectric material on the upper surface of said upper layer and within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is substantially coplanar with the upper surface of said upper layer,

(j) implanting and diffusing into the surface of the substrate source dopants having a second polarity to form a plurality of heavily doped source regions that extend into the substrate along the sides of the trenches;

(k) implanting and diffusing into the surface a plurality of heavily doped body regions having a first polarity, said body regions overlying the drain region in said upper layer; and

(1) forming a metal contact to said body and source regions over the upper surface of said upper layer.

41. (original) The process of claim 40 wherein the depth of the level of the diffused implants for the source regions is substantially coplanar with the level of the conductive gate material in the trenches.